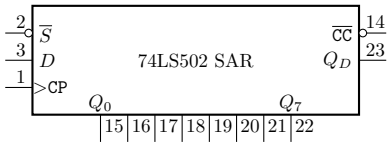
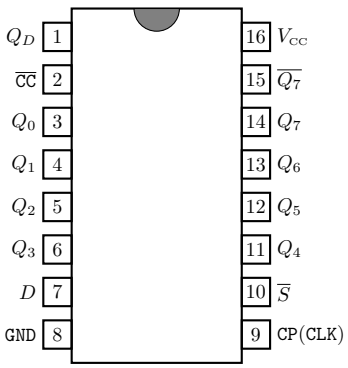
74LS502 SAR Emulator
D. Steck, 6/5/15

This document briefly describes the implementation of an emulator, based on the ATF22V10C CPLD, of the 74LS502 successive-approximation register, formerly available from Fairchild Semiconductor. More details about chip operation are available in Fairchild's original data sheet for the DM74LS502, and more details about this particular emulator can be found online.[1] Files for "burning" the PLD emulator can also be found online.[2]

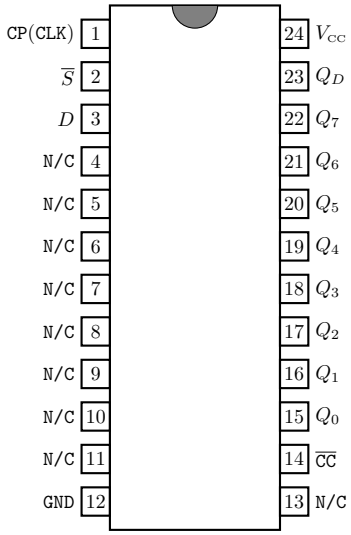
Schematic symbol (emulator); note that $\overline{Q_7}$ functionality is not available in this version:



Pin diagram compared to original:



original 74LS502



74502 emulator

[1] Daniel A. Steck, *Analog and Digital Electronics* (2014), available online at `http://atomoptics-nas.uoregon.edu/~dsteck/teaching/electronics`.

[2] `http://atomoptics-nas.uoregon.edu/~dsteck/teaching/74503`